IN THE DRAWINGS

Please substitute Figs 14a and 14b enclosed herewith for the corresponding Fig. 14 currently on file.

REMARKS

With regard to section 1, 2 and 3 the Examiner has objected to the drawings under 37 C.F.R. 1.83(a). The Applicant cancelled claims 3-10 and has amended Fig. 14 so that the drawings are in compliance with the patent rules.

With regard to sections 3 and 4 the Examiner has rejected claims 2 and 4 under 35 USC 112 second paragraph as being indefinite. Specifically, the Examiner has rejected the term "relatively short length" in claim 2 and "the stripes are relatively short" in claim 4. The applicant has amended claim 2 to replace "relatively short length" with "short length relative to other gates in the CMOS circuit" and cancelled claim 4. A person of ordinary skill in the art would understand that the implied comparison was to other gates with the CMOS circuit. The present amendments make explicit what was previously implicit, consequently such amendment is considered to not add any new matter.

In view of the above claims are considered to comply with 35 USC §112 second paragraph.

With regard to sections 5 and 6, the Examiner has rejected claim 1 under 35 USC 102 (e) as being anticipated by Sidiropoulous et al (US Pat. No. 6,573,779). The Examiner alleges that Sidiropoulous et al teaches all the claimed features in Figs. 3 and 4 and at column 6, line 3. The Applicants respectfully refute the Examiner's contention for at least the following reasons.

To assemble the elements for claim 1, the Examiner alleges teaching of a first gate reference voltage 37. Fig. 3 in fact shows a reference generator 37. A first bias current source 1_{bias} and a device M_{bs1} from Fig. 4 then attributes the operation of buffer 35 of Fig. 3, shown in detail in Fig. 6 to the "device" M_{bs1}. In fact M_{bs2} is connected exactly as shown in Fig. 14b for device 528. And M_{bs1} provides p-channel threshold voltage compensation as its gate is controlled by V_{CM1} the output from reference generator 37. The cited reference is completely silent with regard to the gate size and structure of the device enhancing

sensitivity to process voltage and temperature variations. In fact, the '779 patent teaches at col 6 line 1-2 varying the common mode voltage with V_{TP}, where V_{TP} is defined at col 4 lines 63-65 as the p-channel voltage threshold. Hence, the '779 patent neither teaches nor suggests compensation of bias current for variations in process, voltage, and temperature (PVT).

In view of the above amendments and arguments reconsideration and consequent allowance of claims is respectfully requested.

Applicant hereby petitions for an extension of time to respond to the pending Office Action, and a check for the necessary extension fee is enclosed. If any additional fees are required for this response, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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Dated: 11/9, 2005

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